

Libraries

Name	Process	Form Factor
RGO_GF22_18V18_FDX_45C_CML	FDX	Inline CUP

Summary

The CML library provides a differential current mode logic clock driver to support REFCLK signaling in PCIe applications along with a CML voltage reference cell. Also included is a full complement of power and spacer cells to assemble a CML domain in the pad ring by abutment.

This 22nm library is available in an inline CUP wire bond implementation with a flip chip option.

When using this library with GPIO and other I/O libraries provided by Aragio Solutions, a rail splitter is required to isolate the CML driver in its own power domain. That rail splitter can be obtained from the 1.8V Support: Power library.

ESD Protection:

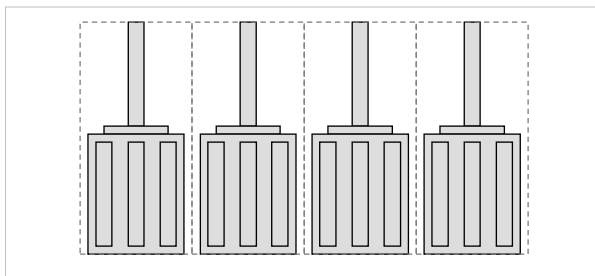
- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

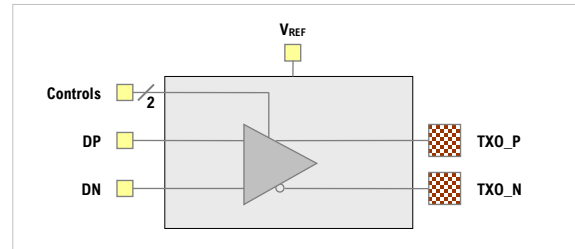
- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

Inline (core-limited) – TBD μm x TBD μm



CMC_OU_100_18V_T: 100MHz CML Clock Driver



CML Differential Clock Driver Features:

- Differential current-mode-logic clock driver with very low jitter
- Target application – PCIe 100 MHz REFCLK
- Typical differential input voltage swing – 0 to 400 mV (referenced to ground)
- Jitter < 3ps @ 100 MHz with ± 100 mV power supply ripple noise
- Common mode voltage (V_{OS}) = 380mV @ 1.5V and 400mV @ 1.8V
- Output-disable and power-down modes
- Powered by 1.5V / 1.8V I/O and 0.8V Core supplies
- Power-up sequencing independent design with Power-On-Control

Recommended operating conditions

Description	Min	Nom	Max	Units
V_{DD} Core supply voltage	0.72	0.80	0.88	V
$V_{D/DD}$ I/O supply voltage	1.62	1.8	1.98	V
T_J Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{DVSS} - 0.3$	-	$V_{D/DD} + 0.3$	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD ^[1]	Temperature
0.8V	FF	0.88	+10%	-40°C
	FF	0.88	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SS	0.72	-10%	-40°C
	SS	0.72	-10%	125°C

[1] DVDD = 1.5V & 1.8V

Cell summary

Name	Description
CMC_OU_100_18V_T *	100 MHz CML Differential clock driver
CMC_RE_000_18V *	CML Voltage reference (VREF)
PLC_VD_PDO_18V *	CML I/O power (DVDD) with POC
PLC_VD_RDO_18V *	CML I/O power (DVDD)
PLC_VS_DRC_18V *	CML I/O ground (VSS)
PLC_VD_RCD_10V *	Core power (VDD)
PLC_VS_DRC_10V *	Core ground (VSS)
SLC_SP_000_18V	0.1µm spacer
SLC_SP_001_18V	1µm spacer
SLC_SP_002_18V	2µm spacer
SLC_SP_005_18V	5µm spacer
SLC_SP_010_18V	10µm spacer

* Vertical-only and horizontal-only orientations

Inline CUP Cells

CUP_GF22_TBD_INLINE	TBD X TBD Inline
CUP_GF22_FC_INLINE	Flip chip with top metal port
CUP_GF22_FC_INLINE_NRV	Flip chip without RV via and RDL port

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